

For Release on May 21, 2007

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**NOVELICS ANNOUNCES MEMQUEST™, A SUITE OF MEMORY COMPILERS
BUILT ON A COMMON PLATFORM THAT CONCURRENTLY EXCELS IN ACTIVE
POWER, LEAKAGE CURRENT, SPEED, PORTABILITY, AND COST**

Aliso Viejo, CA — May 21, 2007 — Novelics, a leading provider of semiconductor embedded memory Intellectual Properties (IPs), today announced the availability of its leading-edge web-based MemQuest™ memory compiler platform. This innovative and unique tool supports Novelics' line of previously announced embedded-memory IPs (e.g., coolSRAM-1T™, coolSRAM-6T™, coolOTP™, coolROM™, coolCACHE™, coolCAM™, and coolREG™), which are implemented in a standard logic CMOS process without requiring any additional masks.

The MemQuest easy-to-use interface allows the System-on-Chip (SoC) designers (1) to explore their entire embedded memory subsystem based on memory types, user-definable operating conditions, area, power, density, speed, etc., on a block-by-block basis, (2) to choose the best optimized memory solution for each block, (3) to compile each memory block independently, (4) to generate all the required industry-standard front- and back-end views, and (5) to easily transfer the entire design files to their desired workstation, independent of the workstation's operating system or hardware, all in a very short time.

"MemQuest™ provides a web-based, easy-to-use, and fast environment for designing all the required memory blocks for our new SoC/ASIC." said Pete Maimone, u-Nav Vice President of Product Development.

"We are pleased to make the MemQuest™ compiler technology available to our customers," said Dr. Cyrus Afghahi, Novelics Chief Executive Officer. "We are committed to growing this unique

memory technology market to enhance productivity and enable system designers to make smart technical decisions without making any unnecessary compromises. For the first time, the low-power design techniques and differentiated IPs (e.g., coolSRAM-1T, coolSRAM-6T, coolCache or coolOTP) can be compiled from a single platform."

"MemQuest is more than just another memory compiler for the SoC/ASIC embedded memory market," said Dr. Gil Winograd, Novelics Chief Operating Officer and Co-Founder. "This leading-edge tool allows a chip designer to architect an entire SoC memory-subsystem as a project with any combination of Novelics' unique memory IPs and customize each memory type or block to suit their overall design requirements."

The Novelics MemQuest memory compiler platform provides support for embedded memory blocks as large as 32Mbits in various geometries (e.g., 180nm, 130nm, 90nm, and 65nm) in collaboration with major Foundries such as TSMC, UMC, SMIC, and SilTerra. The MemQuest™ compiler has been used with leading designs for wireless, TV-Mobile, portable networking, portable multimedia, RFID, and many other complex SoC, ASIC, and ASSP applications.

About Novelics

Novelics, headquartered in Aliso Viejo, California, supplies a portfolio of innovative embedded memory IPs for low-power and high-performance ASIC, ASSP, and SoC designs. Novelics' compiler-driven "cool" and "zero-leakage" Memory IPs include SRAM-1T, SRAM-6T, OTP, high-speed Cache, CAM, and ROM. These differentiated memory IPs are implemented with the standard logic CMOS process with no additional masks or process steps to minimize cost and to maximize reliability and portability. Novelics' customers compete in low-power consumer, wireless, high-speed computing, industrial, and networking applications. For more information, please visit www.novelics.com or email a request to info@novelics.com.

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