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NOVELICS INTRODUCES SILICON-PROVEN coolSRAM-1T™ FOR SOC DESIGNERS WITH LARGE EMBEDDED MEMORY NEEDS

- *coolSRAM-1T™ delivers a 2X reduction in SRAM core size to reduce die size, cost, and power consumption of SOC embedded SRAM*

Aliso Viejo, CA — December 4, 2006 — Novelics, a leading provider of semiconductor embedded memory intellectual property (IP) for low power and high density applications, today announced the availability of its 180 nm and 130 nm *coolSRAM-1T™* products. This IP is available in major foundries. A leading provider of multi-standard semiconductor application-specific integrated circuits for Mobile TV and Digital Audio broadcast standards started production ramp up of chips with the Novelics' embedded coolSRAM-1T™.

SOC designers have successfully used Novelics' differentiated memory IPs such as coolSRAM-1T™, and worked with Novelics seasoned engineering and management team to maximize the value of their industry-leading ICs in designs with over 256 kbits of embedded memory. For example, the Mobile TV customer's SoC can support standards including DVB-H, DMB, ISDB-T and FLO. The company is currently demonstrating their silicon operating without any external memory.

“For this exciting engagement, our fabless ‘Mobile TV’ customer was able to offer an IC that delivers longer battery life and smaller die size as a competitive advantage,” said Cyrus Afghahi, Novelics' Chief Executive Officer. “By working closely with us, our customers will be able to focus on developing their core differentiation and can leverage on our low power and high density memory IPs. ”

“Our target customers compete in low power consumer, video multimedia processors, HDTV, gaming, wireless applications, LCD controller, printer engines, high speed computing, and networking,” said Farzad Zarrinfar, President of Novelics. “We are excited that fabless

semiconductor companies who have leading solutions in explosive markets such as ‘TV enabled cellular phones’ have chosen our technology.”

coolSRAM-1T™ is supported in TSMC’s 180 nm, 130 nm, and 90nm process nodes, in UMC’s 130 nm and 90nm nodes, SMIC’s 90nm, and in Silterra’s 180 nm, and 130 nm nodes. coolSRAM-1T™ is implemented with standard logic CMOS process with no additional masks or process steps, thus minimizing implementation costs, as well as maximizing reliability and portability.

Low Power

The coolSRAM-1T™ memory array has been designed for ultra low power consumption through a combination of techniques to lower active power and leakage power dissipation. The coolSRAM-1T™ does not dissipate any static DC current other than the junction and sub-threshold leakage inherent in any circuit.

coolSRAM-1T™ supports active standby and sleep modes. During sleep mode, the clock and a large percentage of the circuits are suppressed to drastically reduce power dissipation. During standby mode, the memory retains data by using a low frequency refresh operation that dissipates minimal power. The overall architecture and circuits used in coolSRAM-1T™ design result in both low active and low leakage power dissipations. Internal refresh logic is provided as part of the memory array that can transparently provide the refresh, or designers can select an external refresh option if they want to control the refresh externally.

Memory Compiler

A key enabling technology for coolSRAM-1T™ is Novelics’ memory compiler, MemQuest™. This tool enables Novelics’ customers to configure the lowest power, fastest, or most dense coolSRAM-1T™ with the same compiler, thus eliminating potential non-recurring engineering fees for manual implementation. The compiler also enables customers to use the most optimum core size with the shortest time to market. MemQuest™ is based on fully-customized and hand-crafted memory sub-circuits and leaf cells. Therefore, it generates results that are typically within 5% of full custom designs and eliminates manual work in generating memory instances. As a result, the MemQuest™ compiler provides a higher figure of merit (power/speed/density concurrency) than other options.

The coolSRAM-1T™ core memory cell employs a transistor and a structural capacitor to implement the storage cell. In comparison with traditional SRAM, fewer transistors are needed in each cell and thus memory arrays built with coolSRAM-1T™ cells can achieve a 2X reduction in core size vs. arrays based on standard six-transistor memory cells.

coolSRAM-1T™ views including electrical, physical, simulation (Verilog & VHDL), test, and synthesis are all generated by MemQuest™. The Compiler supports insertion of row/column redundancy with minimal timing penalty.

Technical Detail

For more information, technical details, and design methodology guides for coolSRAM-1T™, please contact info@novelics.com or visit www.novelics.com.

About Novelics

Novelics, headquartered in Aliso Viejo, California, supplies a portfolio of innovative embedded memory IPs for low power and high performance ASICs, ASSPs, and SoC designs. Novelics' compiler-driven 'cool' and 'zero-leakage' Memory IPs include OTP, SRAM-1T, SRAM-6T, high Speed Cache, CAM and ROM.

These differentiated memory IPs are implemented with standard logic CMOS process with no additional masks or process steps to minimize cost, as well as maximize reliability and portability.

Our customers compete in low power consumer, industrial, wireless applications, high speed computing and networking. For more information, please visit www.novelics.com or email a request to 'info@novelics.com'.

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